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# NT6868A

## Keyboard Controller

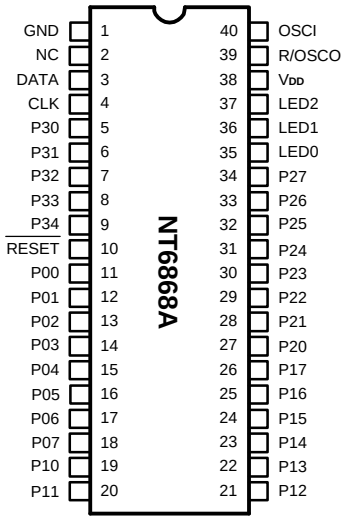
### Features

- Built-in 6502 8-bit CPU
- 2 MHz CPU operation frequency
- 4K bytes of ROM
- 128 bytes of SRAM
- One 8-bit programmable base timer with 1 - 256 µsec interval
- 29 programmable bi-directional I/O pins
- 3 LED direct sink pins with internal serial resistors
- Mask optional for built-in RC oscillator with an external resistor or external ceramic resonator applied
- Watch-dog timer
- Built-in power-on reset
- Built-in low voltage reset
- CMOS technology for low power consumption
- Available in 40 pin DIP package and 40 pad CHIP FORM

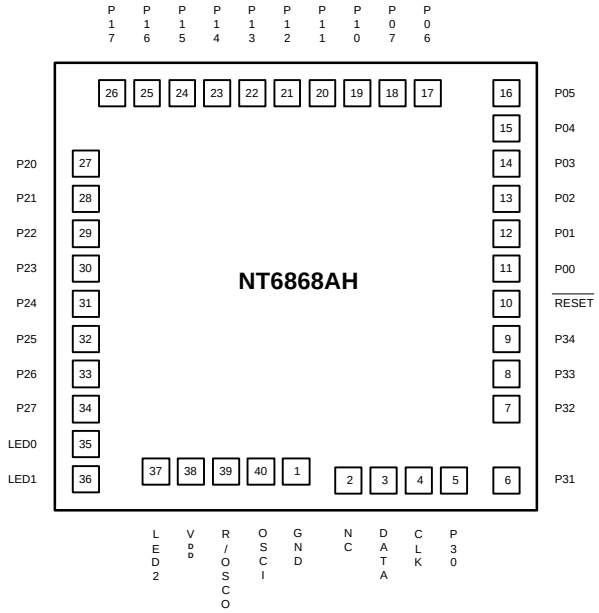
### General Description

NT6868A is a single chip micro-controller for keyboard applications. It incorporates a 6502 8-bit CPU core, 4K bytes of ROM, and 128 bytes of RAM used as working RAM and stack area. It also includes 29 programmable bi-directional I/O pins and one 8-bit pre-loadable base timer. Additionally, it includes a built-in low voltage reset, a 4MHz RC oscillator that requires only a resistor externally applied or a 4MHz ceramic resonator, and a watch-dog timer that prevents system standstill.

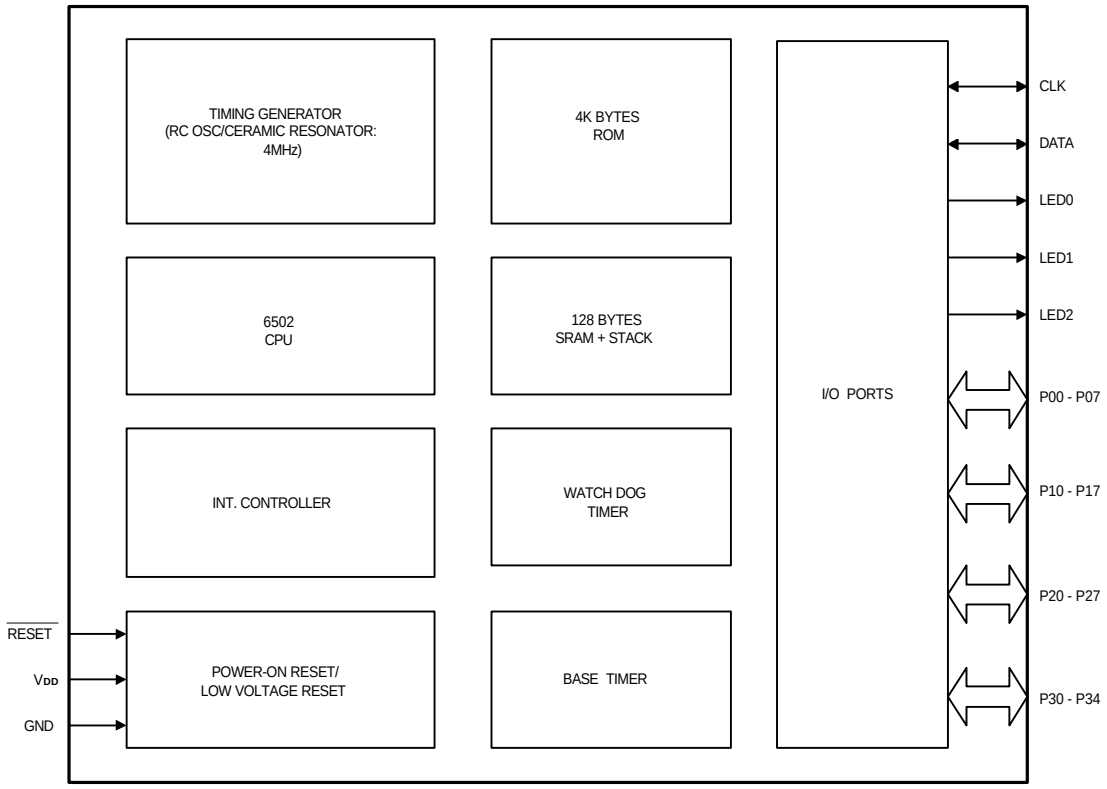
### Pin Configuration




### Pad Configuration



## Block Diagram




## Pin and Pad Descriptions

| Pin No. | Pad No. | Designation | I/O | Description |
|---|---|---|---|---|
| 1 | 1 | GND | P | Ground pin |
| 2 | 2 | NC | - | No connection, recommended to connect $V_{DD}$ or floating |
| 3 | 3 | DATA | I/O | I/O, 10KΩ pull-up resistor for communication |
| 4 | 4 | CLK | I/O | I/O, 10KΩ pull-up resistor for communication |
| 5 - 9,<br>11 - 34 | 5 - 9,<br>11 - 34 | P30 - P34,<br>P00 - P27 | I/O | Bi-directional I/O pins |
| 10 | 10 | $\overline{\text{RESET}}$ | I | $\overline{\text{RESET}}$ signal input pin with internal pull up resistor; Active low |
| 35 - 37 | 35 - 37 | LED0 -<br>LED2 | O | LED direct sink pins |
| 38 | 38 | $V_{DD}$ | P | Power supply |
| 39 | 39 | R/OSCO | I | 47KΩ resistor connected for RC OSC or 4MHz ceramic resonator connected |
| 40 | 40 | OSCI | - | No connection for RC OSC, connected for 4MHz ceramic resonator |

* Under the constraint of the maximum frequency variation, $(\Delta F/F)_{max}$, ≤ ±1%, code 3 (ceramic resonator option) must be selected and pin 39 and pin 40 are connected to a ceramic resonator. If $(\Delta F/F)_{max}$, ≤ ±10%, code 1 (RC OSC option) is recommended to be selected and pin39 connects a 47KΩ resistor with, ≤ ±1% accuracy to $V_{DD}$ and pin 40 is floating.

## Functional Description

### 6502 CPU

6502 is an 8-bit CPU. Refer to 6502 data sheet for details.

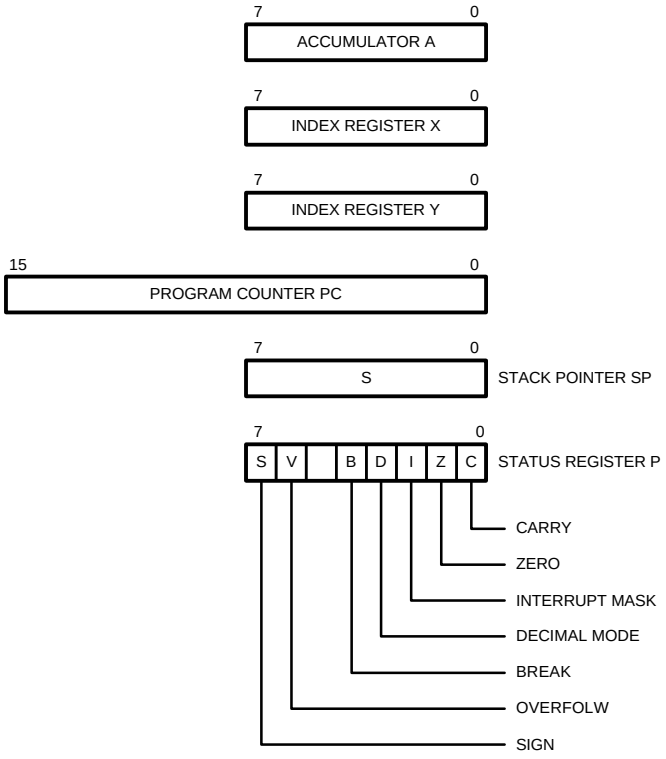



**Figure 1. 6502 CPU Registers and Status Flags**

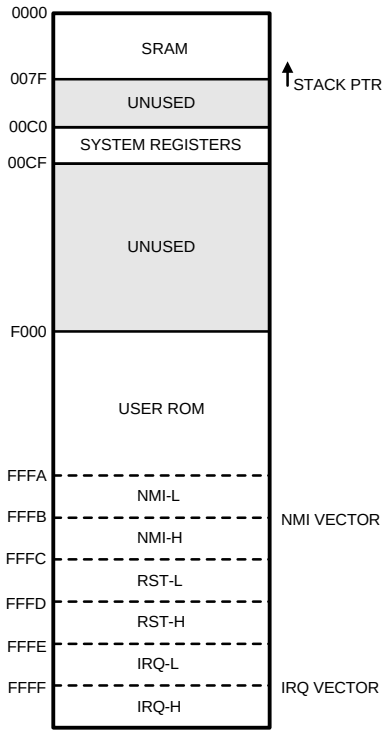



**Figure 2. NT6868A Memory Map**

### System Reserved Registers

| Address | Register | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|---|---|---|---|---|---|---|---|---|---|---|
| $00C0 | BT | BT7 | BT6 | BT5 | BT4 | BT3 | BT2 | BT1 | BT0 | W |
| $00C1 | TCON | - | - | - | - | - | - | - | $\overline{\text{ENBT}}$ | W |
| $00C2 | CLRIRQX | - | - | - | - | - | - | - | CLRIRQTMR | W |
| $00C3 | PORT0 | PD07 | PD06 | PD05 | PD04 | PD03 | PD02 | PD01 | PD00 | RW |
| $00C4 | PORT1 | PD17 | PD16 | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | RW |
| $00C5 | PORT2 | PD27 | PD26 | PD25 | PD24 | PD23 | PD22 | PD21 | PD20 | RW |
| $00C6 | PORT3 | - | - | - | PD34 | PD33 | PD32 | PD31 | PD30 | RW |
| $00C7 | CLK | - | - | - | - | - | - | - | CLK | RW |
| $00C8 | DATA | - | - | - | - | - | - | - | DATA | RW |
| $00C9 | LED | - | - | - | - | - | LED2 | LED1 | LED0 | W |
| $00CA | CLRWDT | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | W |
| $00CB | X | X | X | X | X | X | X | X | X | X |
| $00CC | X | X | X | X | X | X | X | X | X | X |
| $00CD | X | X | X | X | X | X | X | X | X | X |
| $00CE | X | X | X | X | X | X | X | X | X | X |
| $00CF | X | X | X | X | X | X | X | X | X | X |

- : no effect  X : access not allowed

### 4K X 8 ROM

The built-in ROM program code, executed by the 6502 CPU, has a capacity of 4K X 8 bits and is addressed from F000H to FFFFH.

### 128 X 8 SRAM

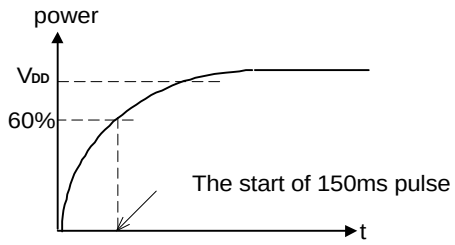
The built-in SRAM is used for general purpose data memory and for the stack area. SRAM is addressed from 0000H to 007FH. User can allocate stack area in the SRAM by setting stack pointer register (S). Because the 6502C default stack pointer is 01FFH, it must be mapped to 007FH. Mapping from 01XX to 00XX is done internally by setting the S register to 7FH via software programming.

For example :

```
LDX   #$7F
TXS
```

### Power-On Reset

Built-in power-on reset circuit can generate a 150ms pulse to reset the entire chip. The beginning of the 150ms pulse occurs at 60% of $V_{DD}$ when powered on.



## Timing Generation

This block generates the system timing and control signal supplied to CPU and on-chip peripherals. There are two types of system clock sources: built-in RC oscillator or external ceramic resonator. Both of them are mask optional and generate a 4MHz system clock. They also generates 2MHz for CPU, and 1MHz for base timer. The following shows the relationship of code type number and oscillation type.

| Oscillator Type | Code Number |
|---|---|
| RC OSC | 1 |
| Ceramic Resonator | 3 |

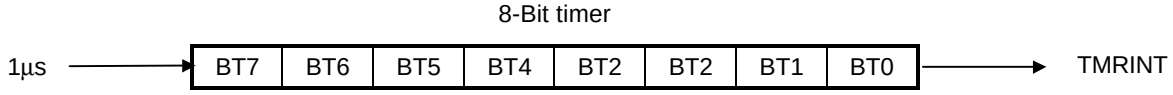
The following table provides the relationship between external resistor and RC OSC frequency. (for reference only)

| External Resistor (KW) | RC OSC Frequency (MHz) |
|---|---|
| 39 | 4.7 |
| 43 | 4.44 |
| 47 | 4 |
| 56 | 3.68 |

## Base Timer

The base timer is an 8-bit counter with a 1MHz clock source. The base timer can be enabled/disabled by CPU. After reset, the base timer is disabled and cleared. The base timer can be preset by writing BT7 - BT0 to the BT register at any time. When enabled, the base timer starts counting from the preset value. When the value reaches FFH, it generates a timer interrupt if the timer interrupt is enabled. When it reaches the maximum value of FFH, the base timer will wrap around and begin counting at 00H. The timer interval can be programmed from 1 - 256 μsec. The base timer can be enabled by writing a '0' to '$\overline{\text{ENBT}}$' in the TCON (Timer Control) register. The $\overline{\text{ENBT}}$ is a level trigger.

Base timer structure:




BT pre-load data:

| Addr. | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|---|
| $00C0 | BT | BT7 | BT6 | BT5 | BT4 | BT3 | BT2 | BT1 | BT0 | (W) |

Timer Control Regisrer:

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $00C1 | TCON | - | - | - | - | - | - | - | $\overline{\text{ENBT}}$ | (W) |

## INT. Controller

When BASE TIMER overflow occurs, it will set the IRQTMR flag. The IRQTMR flag cannot be directly accessed by software. Once set by an interrupt source, it remains High unless cleared by writing '1' to the corresponding bit in CLRIRQX ($00C2H). This register is cleared to '0' on initialization by system reset.
When an interrupt occurs, CPU jumps to $FFFEH & $FFFFH to execute the interrupt service routine. When BASE TIMER interrupt occurs and enters the interrupt service routine, the IRQTMR flag must be cleared by software.

Interrupt Control Register:

| Addr. | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|---|
| $00C2 | CLRIRQX | - | - | - | - | - | - | - | CLRIRQTMR | (W) |

## I/O Ports

The NT6868A has 31 pins dedicated to input and output. These pins are grouped into 6 ports, as follows:

PORT 0 (P00 - P07):

Port 0 is an 8-bit bi-directional CMOS I/O port that is internally pulled High by PMOS. Each pin of port 0 can be bit programmed as an input or output pin under the software control. When programmed as output, data is latched to the port data register and output to the pin. Port 0 pins with "1" written to them are pulled high by the internal PMOS pull-ups, and are used as inputs in that state. These input signals can then be read. The port output is High after reset.

PORT 1 ( P10 - P17 ) : Functions the same as PORT 0.

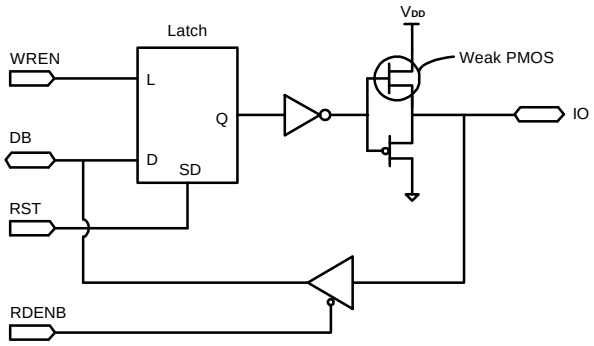
PORT 2 ( P20 - P27) : Functions the same as PORT 0.

PORT 3 ( P30 - P34) : Functions the same as PORT 0.

CLK & DATA : These two pins have the same structure as I/O ports, except for the 10KΩ internal pull-ups.

PORT Registers:

| Addr. | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|---|
| $00C3 | PORT0 | PD07 | PD06 | PD05 | PD04 | PD03 | PD02 | PD01 | PD00 | (RW) |
| $00C4 | PORT1 | PD17 | PD16 | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | (RW) |
| $00C5 | PORT2 | PD27 | PD26 | PD25 | PD24 | PD23 | PD22 | PD21 | PD20 | (RW) |
| $00C6 | PORT3 | - | - | - | PD34 | PD33 | PD32 | PD31 | PD30 | (RW) |
| $00C7 | CLK | - | - | - | - | - | - | - | CLK | (RW) |
| $00C8 | DATA | - | - | - | - | - | - | - | DATA | (RW) |

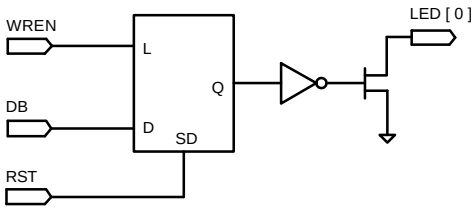



**IO Port Structure**

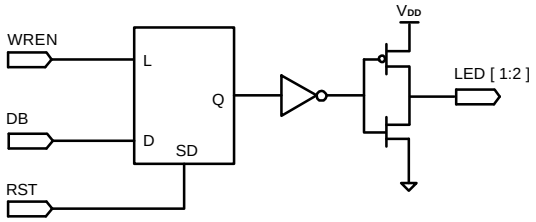
### LED Port

There are 3 LED direct sink pins which require no external serial resistors. The address is mapped to address $00C9.

| Addr. | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|---|
| $00C9 | LED | - | - | - | - | - | LED2 | LED1 | LED0 | (W) |




**LED0 Port Structure**




**LED1, LED2 Port Structures**

### Watch-Dog Timer

NT6868A implements a watch-dog timer, which protects programs against system standstill. The clock of the watch-dog timer is derived from the on-chip RC oscillator. The watch-dog timer interval is about 0.175 of a second. The timer must be cleared within every 0.175 second during normal operation; otherwise, it will overflow and cause a system reset. The watch-dog timer is cleared and enabled after a system reset. It cannot be disabled by software. The user can clear the watch-dog timer by writing #55H to CLRWDT ($00CAH) register.

For example:

```
LDA     #$55
STA     $00CA
```

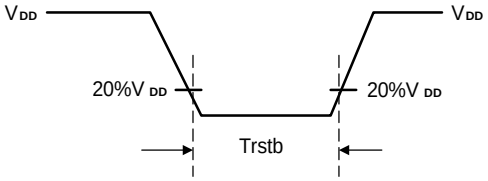
| Addr. | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|---|
| $00CA | CLRWDT | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | (W) |

### Low Voltage Reset (LVR) Circuit

The NT6868A will check on the voltage level of power supply. When the voltage level of power supply is below a threshold of 3.0V (Typical), the LVRC will issue a reset output to the chip until the power voltage level is above the threshold voltage of 3.0V (Typical) again. As soon as the power voltage arises to 3.0V (Typical), the entire chip will be reset for about 150ms.

### $\overline{\text{RESET}}$

NT6868A can also be externally reset via $\overline{\text{RESET}}$ pin. A reset is initiated when the signal at the $\overline{\text{RESET}}$ pin is held Low for at least 10 system clock. As soon as $\overline{\text{RESET}}$ signal goes high, the NT6868A begins to be reset for about 150ms. The following shows the definition of $\overline{\text{RESET}}$ input low pulse width.



### Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input/Output Voltage . . . . . .GND -0.2V to $V_{DD}$ + 0.2V

Operating Ambient Temperature . . . . . .0°C to +70°C

Storage Temperature . . . . . .-55°C to +125°C

Operating Voltage ($V_{DD}$) . . . . . .+4.5V to 5.5V

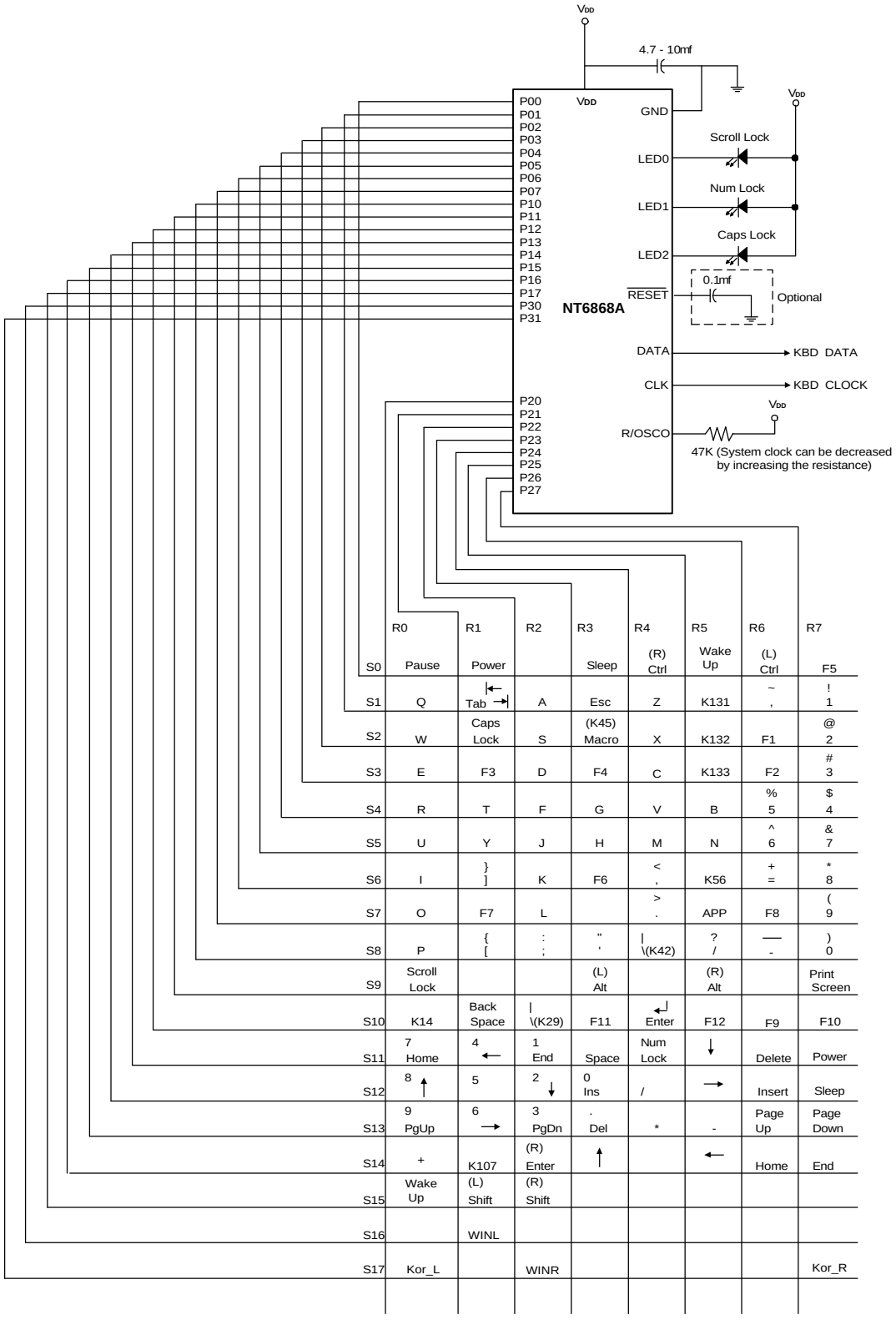
### *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

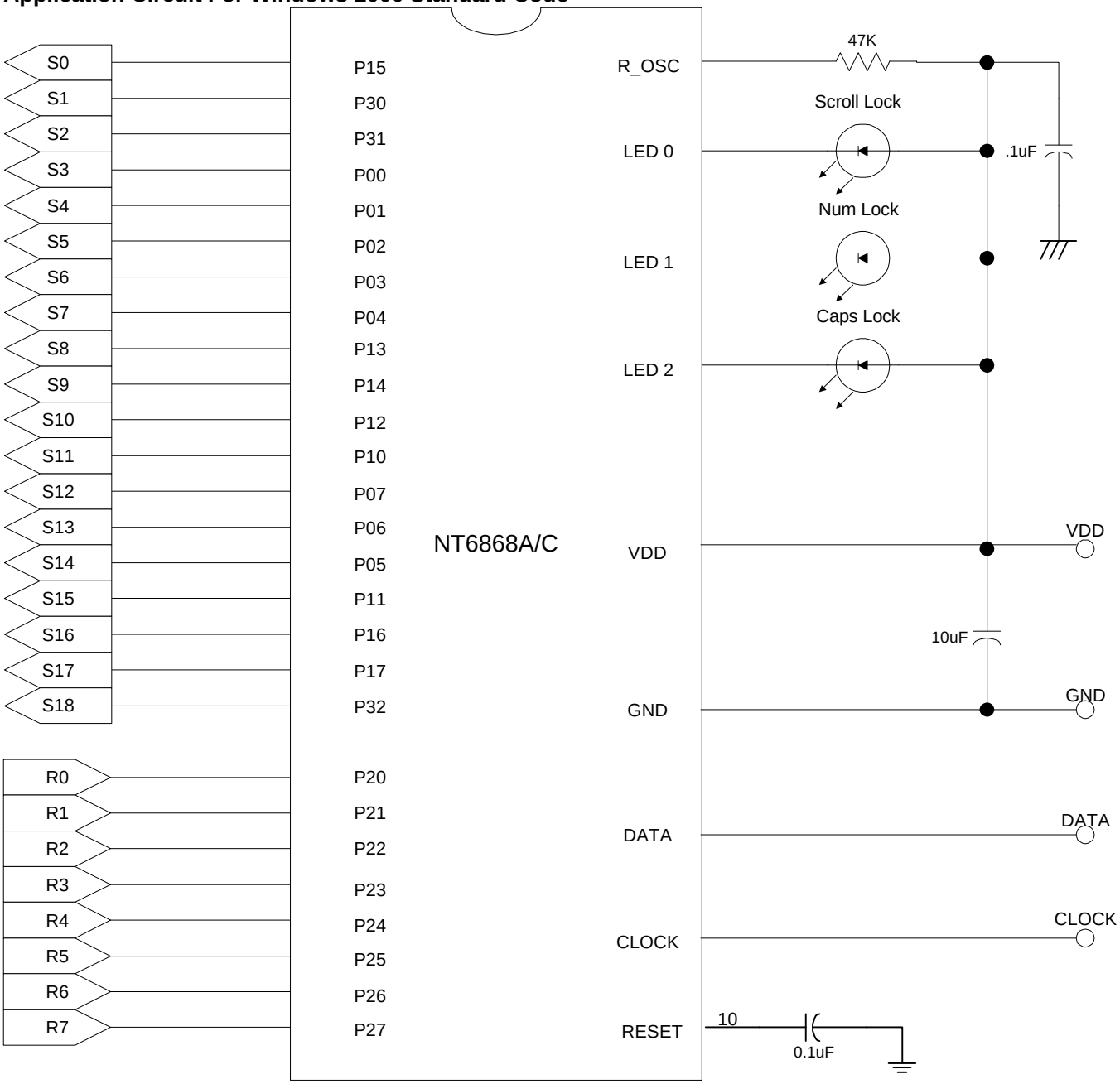
**DC Electrical Characteristics** ($V_{DD}$ = 5V, GND = 0V, $T_A$ = 25°C, Fosc = 4MHz, unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current | | | 20 | mA | No load |
| $V_{IH}$ | Input High Voltage | 2 | | | V | |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | |
| $V_{OH1}$ | Output High Voltage (Port 0, 1, 2, 3) | 2.4 | | | V | $I_{OH}$ = -100μA |
| $V_{OH2}$ | Output High Voltage (CLK, DATA) | 2.4 | | | V | $I_{OH}$ = -400μA |
| $V_{OL1}$ | Output Low Voltage (PORT 0, 1, 2) | | | 0.4 | V | $I_{OL}$ = 4mA |
| $V_{OL2}$ | Output Low Voltage (PORT 3) | | | 0.4 | V | $I_{OL}$ = 5mA |
| $V_{OL3}$ | Output Low Voltage (CLK, DATA) | | | 0.4 | V | $I_{OL}$ = 10mA |
| ΔF/F | Initial Frequency Variation 1 | | | +/-10 | % | For RC OSC option only; By Lots |
| ΔF/F | Frequency Variation 2 | | | +/-1 | % | For ceramic resonator option only; By Lots |
| $I_{LED}$ | LED Sink Current (LED 0, 1, 2) | 10 | 14 | 17 | mA | $V_{OL}$ = 3.2V |
| $V_{LVR}$ | Low Voltage Reset Threshold | | 3.0 | | V | |
| $T_{POR}$ | Power-on Reset Time | 120 | 150 | 180 | ms | |
| $T_{RSTB}$ | $\overline{\text{RESET}}$ Input Low Pulse Width | 2.5 | | | μs | 10 system clocks |
| $R_{PH}$ | $\overline{\text{RESET}}$ Pull High Resistor | | 220 | | KΩ | |

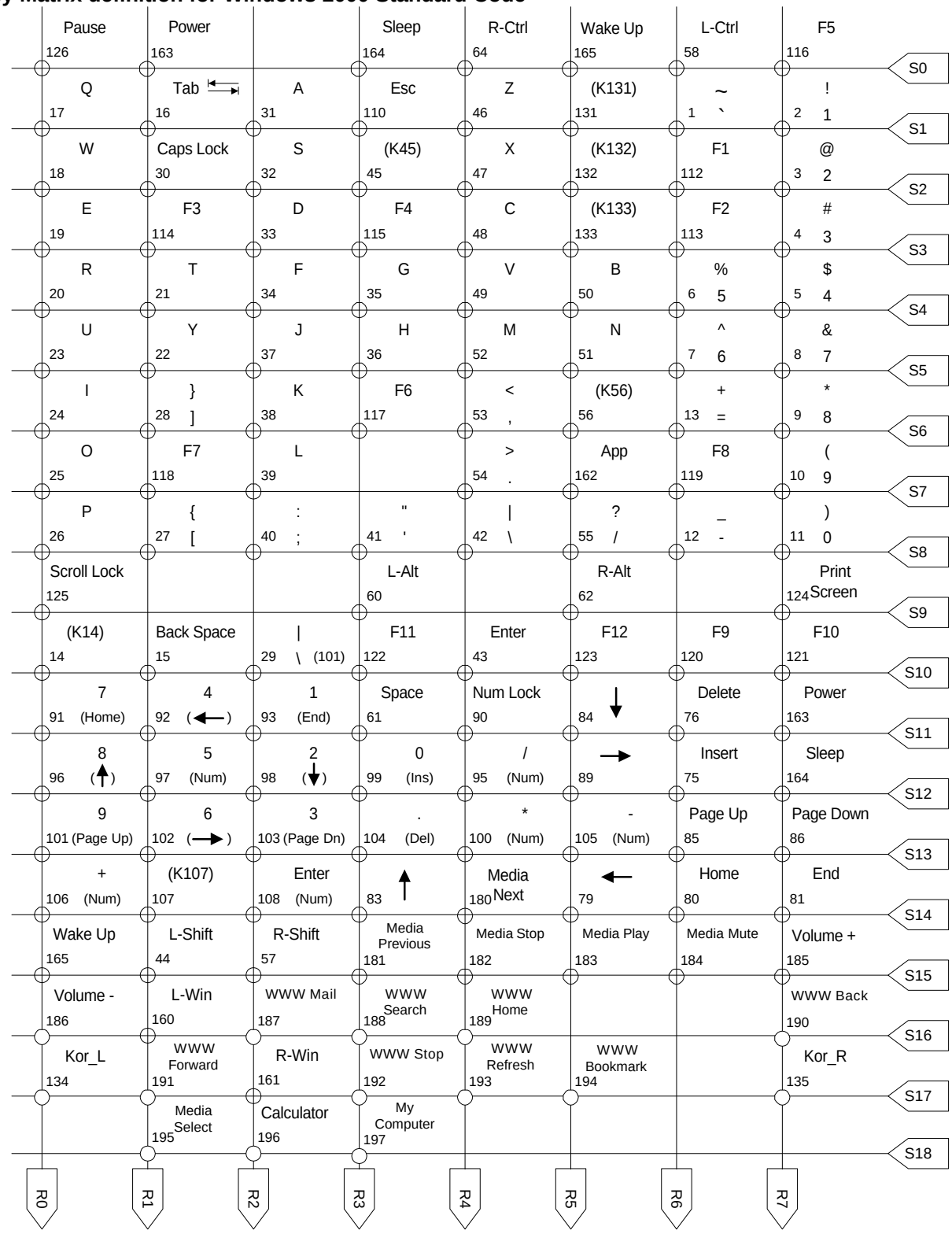
**Application Circuit For Windows 98 Keyboard** (for reference only)



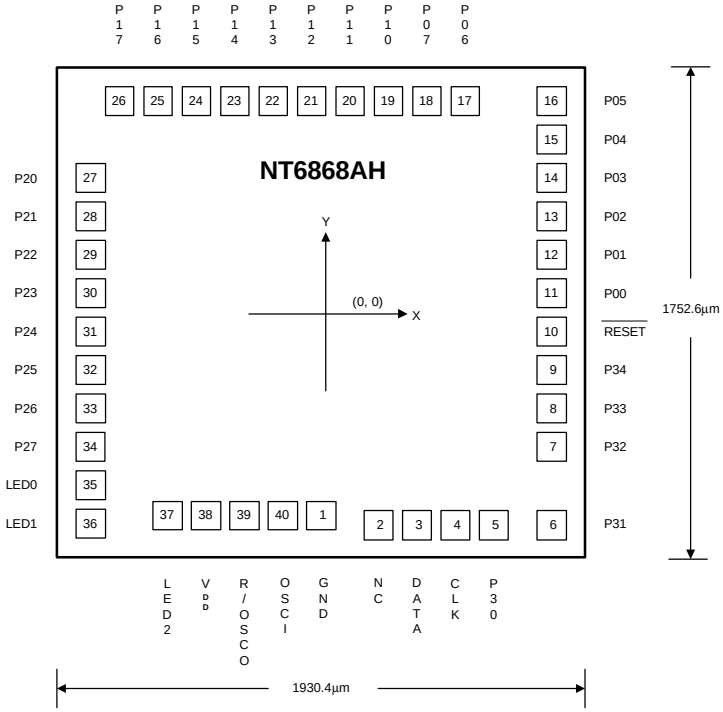
**Application Circuit For Windows 2000 Standard Code**



## Key Matrix definition for Windows 2000 Standard Code



## Bonding Diagram




*Substrate Connect to $V_{DD}$ or Keep Floating

unit: μm

| Pad No. | Designation | X | Y | Pad No. | Designation | X | Y |
|---|---|---|---|---|---|---|---|
| 1 | GND | -74.4 | -712.1 | 21 | P12 | -93.9 | 727.5 |
| 2 | NC | 55.6 | -727.5 | 22 | P13 | -223.9 | 727.5 |
| 3 | DATA | 185.6 | -727.5 | 23 | P14 | -353.9 | 727.5 |
| 4 | CLK | 445.6 | -727.5 | 24 | P15 | -483.9 | 727.5 |
| 5 | P30 | 575.6 | -727.5 | 25 | P16 | -613.9 | 727.5 |
| 6 | P31 | 812.9 | -728.1 | 26 | P17 | -756.4 | 727.5 |
| 7 | P32 | 818.1 | -460.6 | 27 | P20 | -818.2 | 519.3 |
| 8 | P33 | 818.1 | -330.6 | 28 | P21 | -818.2 | 389.3 |
| 9 | P34 | 818.1 | -200.6 | 29 | P22 | -818.2 | 259.3 |
| 10 | $\overline{\text{RESET}}$ | 818.1 | -70.6 | 30 | P23 | -818.2 | 129.3 |
| 11 | P00 | 818.1 | 59.4 | 31 | P24 | -818.2 | -0.7 |
| 12 | P01 | 818.1 | 189.4 | 32 | P25 | -818.2 | -130.7 |
| 13 | P02 | 818.1 | 319.4 | 33 | P26 | -818.2 | -260.7 |
| 14 | P03 | 818.1 | 449.4 | 34 | P27 | -818.2 | -390.7 |
| 15 | P04 | 818.1 | 579.4 | 35 | LED0 | -818.2 | -520.7 |
| 16 | P05 | 818.1 | 721.9 | 36 | LED1 | -818.2 | -666.8 |
| 17 | P06 | 426.1 | 727.5 | 37 | LED2 | -594.4 | -661.6 |
| 18 | P07 | 296.1 | 727.5 | 38 | $V_{DD}$ | -464.4 | -661.6 |
| 19 | P10 | 166.1 | 727.5 | 39 | R/OSCO | -334.4 | -661.6 |
| 20 | P11 | 36.1 | 727.5 | 40 | OSCI | -204.4 | -661.6 |

## Ordering Information

| Part No. | Package |
|---|---|
| NT6868AH | CHIP FORM |
| NT6868A | 40L DIP |

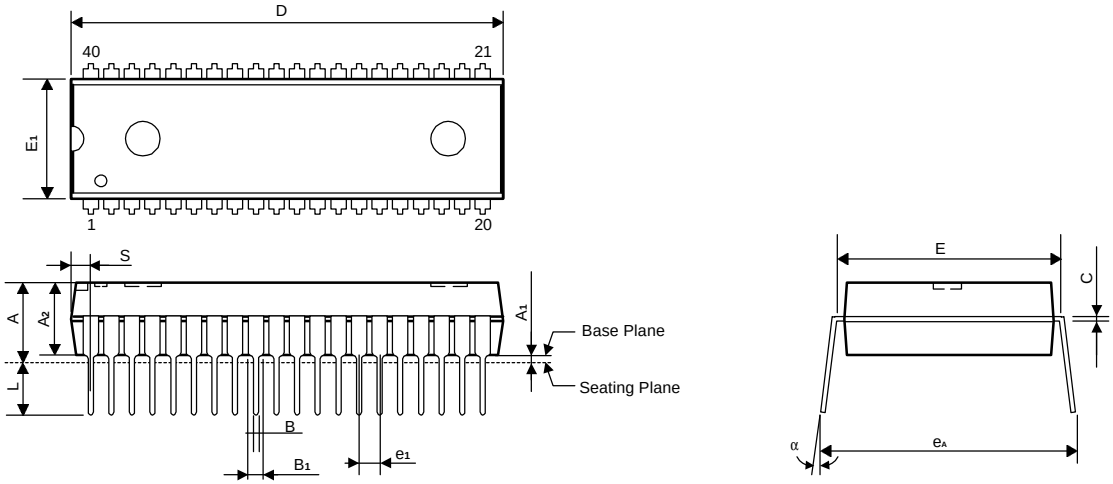
| Code Type No. | Oscillation Type |
|---|---|
| 1 | Built-in RC OSC |
| 3 | Ceramic Resonator |

| Function | Package Type | Order Information |
|---|---|---|
| Windows 95 keyboard | DIP | NT6868A-0011 |
| | COB | NT6868AH-0046 |
| Windows 98 keyboard | DIP | NT6868A-10100 |
| | COB | NT6868AH-10088 |

## Package Information

### DIP 40L Outline Dimensions

unit: inches/mm




| Symbol | Dimensions in inches | Dimensions in mm |
|---|---|---|
| A | 0.210 Max. | 5.33 Max. |
| $A_1$ | 0.010 Min. | 0.25 Min. |
| $A_2$ | 0.155±0.010 | 3.94±0.25 |
| B | 0.018 +0.004 -0.002 | 0.46 +0.10 -0.05 |
| $B_1$ | 0.050 +0.004 -0.002 | 1.27 +0.10 -0.05 |
| C | 0.010 +0.004 -0.002 | 0.25 +0.10 -0.05 |
| D | 2.055 Typ. (2.075 Max.) | 52.20 Typ. (52.71 Max.) |
| E | 0.600±0.010 | 15.24±0.25 |
| $E_1$ | 0.550 Typ. (0.562 Max.) | 13.97 Typ. (14.27 Max.) |
| $e_1$ | 0.100±0.010 | 2.54±0.25 |
| L | 0.130±0.010 | 3.30±0.25 |
| α | 0° ~ 15° | 0° ~ 15° |
| $e_A$ | 0.655±0.035 | 16.64±0.89 |
| S | 0.093 Max. | 2.36 Max. |

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension $E_1$ does not include resin fins.
3. Dimension S includes end flash.